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Physics Letters A 323 (2004) 16–21
PHYSICS LETTERS A
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Can single electron logic microprocessors work at room temperature? ☆

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Received 26 September 2003; received in revised form 9 December 2003; accepted 9 December 2003

Communicated by C.R. Doering

Abstract

The error rate of single electron logic based on single electron transistors (SETs) at nonzero temperature has been estimated. Similarly to recent microelectronic studies [Phys. Lett. A 305 (2002) 144], the maximal error rate of one bit-flip-error chip^{-1} year^{-1} is used as the condition of the error-free performance. The aspects of power dissipation and error-free performance are studied versus the radius of quantum dot (QD). The conclusion is that microprocessors with silicon QDs of less than 1 nm radius can be used at room temperature.

1. Introduction

During the last decade single electron tunneling at ultra-small junction has received a great deal of attention in nanoelectronics. Two pre-requirements for the satisfactory on/off switching operation of a single ultrasmall junction are related to the capacitance, C, and the tunneling resistance, R_T, of the junction [2,3]. Firstly, the tunneling resistance of the ultrasmall junction has to be much greater than the resistance quantum $R_K = h/e^2 \cong 25.8$ kΩ. This condition is required since the energy uncertainty associated with the tunneling lifetime, $\tau_T = R_T C$, should be much smaller than the electrostatic charging energy $E_C = e^2/2C$. Secondly, the electrostatic charging energy should be much greater than the thermal fluctuation energy, which requirement results in

$$C \ll e^2/k_B T, \tag{1}$$

where k_B is the Boltzmann constant and T is the temperature. The first condition leads to the required discrete energy levels for single electron tunneling, and the second one to the blockade of the thermally assisted tunneling. The single electron tunneling has been observed at very low temperatures (< 4 K) [4], where both requirements are easily satisfied by today's technology. A variety of single electron tunneling devices—electrometers, transistors, sensors, etc. [4–7], have been reported to successfully operate at low temperatures, as a single switching device.

In single electron microprocessors, logic levels are dependent on a single electron. Averin and Likharev

☆ This is a revised version of the talk presented at the First International Symposium on Fluctuations and Noise, Santa Fe, June 2003, published in [Proc. SPIE Int. Soc. Opt. Eng. 5115 (2003) 174].

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0375-9601/$ – see front matter
doi:10.1016/j.physleta.2003.12.048

[8], and Korotkov [9] proposed single electron logic gates and circuitry. They used the SET as the basic component of these circuits. However, at non-zero temperature, thermally assisted tunneling takes place even at such bias/control voltages where the device would have closed at zero temperature [8]. Apparently, this phenomenon leads to bit flip errors.

In this article, the maximal error rate of one bit-flip-error chip^{-1} year^{-1} or alternatively one bit-flip-error transistor^{-1} year^{-1} is used as the condition of the error-free performance. In single electron logic chips, this limit corresponds to one electron chip^{-1} year^{-1}.

2. Error-free performance condition

We consider a SET, with double single electron junction, including a gate capacitor and a QD, with low impedance driving and outputting, i.e., $Z_1, Z_2, Z_G \ll R_K, \omega^{-1}C_1^{-1}, \omega^{-1}C_2^{-1}, \omega^{-1}C_G^{-1}$, as shown in Fig. 1. Under these low-impedance conditions, the single electron tunneling rate through each junction is expressed as follows [10,11]:

$$\vec{\Gamma}_1 = \frac{1}{e^2R_1}\frac{E_{1r}(V,V_G,ne)}{1-\exp[-\beta E_{1r}(V,V_G,ne)]} = \frac{k_BT}{e^2R_1}\frac{\eta_{1r}}{1-\exp(-\eta_{1r})}, \tag{2a}$$

$$\overleftarrow{\Gamma}_1 = \frac{1}{e^2R_1}\frac{E_{1l}(V,V_G,ne)}{\exp[\beta E_{1l}(V,V_G,ne)]-1} = \frac{k_BT}{e^2R_1}\frac{\eta_{1l}}{\exp(\eta_{1l})-1}, \tag{2b}$$

$$\vec{\Gamma}_2 = \frac{1}{e^2R_2}\frac{E_{2r}(V,V_G,ne)}{1-\exp[-\beta E_{2r}(V,V_G,ne)]} = \frac{k_BT}{e^2R_2}\frac{\eta_{2r}}{1-\exp(-\eta_{2r})}, \tag{2c}$$

$$\overleftarrow{\Gamma}_2 = \frac{1}{e^2R_2}\frac{E_{2l}(V,V_G,ne)}{\exp[\beta E_{2l}(V,V_G,ne)]-1} = \frac{k_BT}{e^2R_2}\frac{\eta_{2l}}{\exp(\eta_{2l})-1}, \tag{2d}$$

where $\vec{\Gamma}$ and $\overleftarrow{\Gamma}$ are the single electron tunneling rates through the junction in a left-to-right and a right-to-left directions, respectively. The subscript number represents the different junctions, and the subscripts r and l represent the direction that an electron tunnels from left to right and from right to left, respectively.

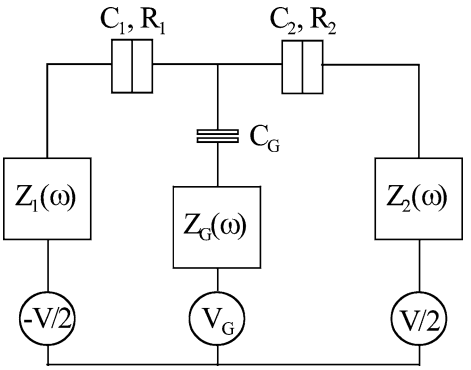

Fig. 1. Single electron tunneling transistor with driving impedances. The tunneling resistances and capacitances of the double junction are R_1, C_1 and R_2, C_2, respectively. C_G is the gate capacitance. The Z_is are the generator impedances of the driving (Z_1 and Z_G) and the output (Z_2).

R is the tunneling resistance, $\beta = 1/k_BT$, and n is the number of the excess charge on the QD. The tunneling-related energies in Eq. (2) are defined by

$$E_{1r}(V,V_G,ne) = \frac{e}{C_\Sigma}\left[\left(C_2+\frac{C_G}{2}\right)V + C_GV_G + ne - \frac{e}{2}\right], \tag{3a}$$

$$E_{1l}(V,V_G,ne) = \frac{e}{C_\Sigma}\left[\left(C_2+\frac{C_G}{2}\right)V + C_GV_G + ne + \frac{e}{2}\right], \tag{3b}$$

$$E_{2r}(V,V_G,ne) = \frac{e}{C_\Sigma}\left[\left(C_1+\frac{C_G}{2}\right)V - C_GV_G - ne - \frac{e}{2}\right], \tag{3c}$$

$$E_{2l}(V,V_G,ne) = \frac{e}{C_\Sigma}\left[\left(C_1+\frac{C_G}{2}\right)V - C_GV_G - ne + \frac{e}{2}\right], \tag{3d}$$

and the dimensionless energies η's are defined by

$$\eta_i(V,V_G,ne) = \beta E_i(V,V_G,ne) = \frac{E_i(V,V_G,ne)}{k_BT} \quad (i = 1r,\ 1l,\ 2r \text{ and } 2l). \tag{4}$$

Here, C_Σ is the sum of the capacitances, $C_\Sigma = C_1 + C_2 + C_G$. Eq. (2) shows that the tunneling rate depends only on the dimensionless energy, η_i, and the tunneling resistance at fixed temperature. At a given tunneling resistance and temperature Eq. (4) allows us to draw the different regimes of working, as shown in Fig. 2 as a function of the source-drain voltage, V, and the gate voltage, V_G. The maximal error rate $\Gamma^0_{SET} =$

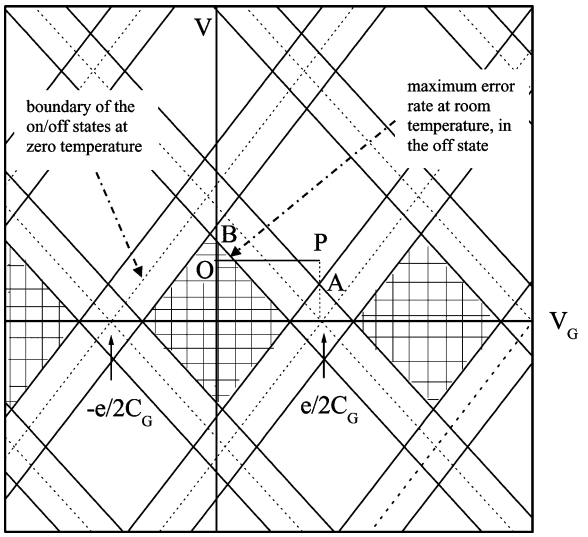

Fig. 2. Working regimes of the SET with asymmetric junctions. With symmetric junctions, the figures would be symmetric on the axes. The dotted lines represent the boundaries between the "on" and "off" states at zero temperature, while the solid lines represent the conditions of the maximal error rate in the "off" state at room temperature. Point O and P represent "off" and "on" states.

3.17×10^{-8} Hz, which corresponds to the limit of one bit-flip-error transistor^{-1} year^{-1}, is used as the condition of the error-free performance [12] on Fig. 2. The dotted lines represent the boundaries between the "on" and "off" states at zero temperature, while the solid lines represent the conditions of the maximal error rate in the "off" state. Each region represents different tunneling combination. The checked regions represent the zero current regions, defined by the maximal error rate, and their area is temperature dependent (see Eq. (4)). These regions exist if the following conditions are satisfied simultaneously:

$$\eta_{jr}(V, V_G, ne) \leqslant -\alpha_j^r(R_j, T),$$
$$\eta_{jl}(V, V_G, ne) \geqslant \alpha_j^l(R_j, T), \tag{5}$$

where we call the α's stability parameters. Eqs. (3), (4) and relations (5) are used to generate Fig. 2.

It is important to note here that in order to have a reasonable estimation of the α's used in Eq. (5), we have proceeded in the following way. The actual values of the α's can be obtained from the following

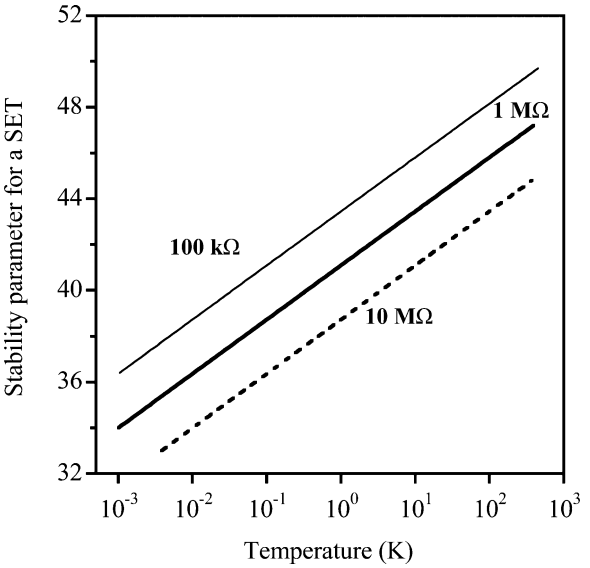

Fig. 3. Stability parameter as a function of temperature. It is evaluated by using Eq. (6).

equations:

$$\frac{\Gamma_{\mathrm{SET}}^0 e^2 R_j}{k_B T} = \frac{-\alpha_j^r(R_j, T)}{1 - \exp[\alpha_j^r(R_j, T)]}, \tag{6a}$$

or using the backward tunneling rate:

$$\frac{\Gamma_{\mathrm{SET}}^0 e^2 R_j}{k_B T} = \frac{\alpha_j^l(R_j, T)}{\exp[\alpha_j^l(R_j, T)] - 1} \quad (j = 1, 2), \tag{6b}$$

where Eqs. (6a) and (6b) are relevant to the different tunneling direction and they give the same result for the α's. Fig. 3 shows the dependence of the stability parameter on temperature at the different tunneling resistance. It shows that although the α's are implicit functions of the tunneling resistance and temperature, they can be approximated by the following semiempirical way:

$$\alpha(R_j, T) \cong \ln \alpha(R_j, T) - \ln\left(\frac{\vec{\Gamma}^Y e^2 R_j}{k_B T}\right)$$
$$\cong \bar{\alpha} - n \ln\left(\frac{R_j}{10^6 T}\right), \tag{7}$$

where $\bar{\alpha} = 41.1$ and $n = 1.025$ for a single SET.[1] After substituting the α obtained from Eq. (7) into Eq. (5),

[1] The stability parameter also depends on the number N of the SETs in a chip since the error rate is proportional to N.

the error-free zero current condition is obtained from Eqs. (3), (4), (5) and (7):

$$\frac{e^2}{2C_\Sigma} > \alpha(R_T, T)k_B T. \tag{8}$$

Eq. (8) expresses the condition of having the tunneling rate below the maximal error rate in the "off" state.

At practical operation the V and V_G has to satisfy two different kinds of requirements [1]. First, the drain voltage cannot be greater than V^{max} which corresponds to the maximal error rate in the "off" state. Second, in the "on" state, the gate should be driven by V_G^{opt} which provides the maximal possible current at given V^{max}. In Ref. [1], simple considerations based on Eqs. (3) lead to

$$V^{max} = \min\left\{ \frac{2}{2C_1 + C_G}\left(\frac{e}{2} - \frac{\alpha_1^r C_\Sigma k_B T}{e}\right), \frac{2}{2C_2 + C_G}\left(\frac{e}{2} - \frac{\alpha_1^r C_\Sigma k_B T}{e}\right)\right\} \tag{9a}$$

and

$$V_G^{opt} = \frac{e}{2C_G} + \left[(2C_1 + C_G)\alpha_1 - (2C_2 + C_G)\alpha_2\right]k_B T \times [2eC_G]^{-1}, \tag{9b}$$

where $\alpha_j = \alpha(R_j, T)$ and $\min(a, b)$ represents the minimum of a and b. If the two junctions are symmetric, i.e., $C_1 = C_2$, $R_1 = R_2 = R$, then Eqs. (9) will be simplified so that the operation voltages in the "on" state become $V^{max} = e/2C_\Sigma$ and $V_G^{opt} = e/2C_G$. In this case, we have the maximal rate of electron flow through the device:

$$\vec{\Gamma}_t = \frac{1}{8C_\Sigma R[1 - \exp(-\beta e^2/4C_\Sigma)]} \cong \frac{1}{8C_\Sigma R}. \tag{10}$$

Eq. (10) is based on unidirectional tunneling because tunneling in the reverse direction would be negligible at the maximal tunneling rate conditions.

When the transistor runs at the maximal clock frequency, the dissipation power of a single SET with symmetric junctions is

$$P_1 = e \cdot \vec{\Gamma}_t \cdot V_G^{opt} = \frac{e^2}{16C_G C_\Sigma R}. \tag{11}$$

The maximal error rate for the chip with N SETs is one bit-flip-error chip^{-1} year^{-1}, i.e., $\Gamma^0_{chip} = \Gamma^0_{SET}/N$. For a chip with 10^9 SETs, we get $\alpha_{10^9} \cong 1.025\ln(10^6/R_T T) - 62.25$.

It is important to note that this is the ultimate lower limit of dissipation because Eq. (11) takes into the account only the energy needed to control the device. The actual power dissipation of the device is not included in this picture because it can be dependent on several other conditions.

3. Size-dependence

In general, the semiconductor SET is built in lateral structure which has 2-dimensional electron gas. In the lateral structure, the QD of the SET is supposed to be a flat circular disk. Therefore, using the size dependence of the geometric capacitance, $C_\Sigma = 8\varepsilon R_{QD}$ [13], we obtain the following relations for the size dependence of the error-free performance condition:

$$R_{QD} \leqslant \frac{e^2}{16\varepsilon\alpha(R, T)k_B T}, \qquad \vec{\Gamma} \cong \frac{1}{64\varepsilon R_{QD} R}, \qquad P_1 = \frac{e^2}{128\varepsilon C_G R_{QD} R}, \tag{12}$$

where ε is the permittivity of insulator and R_{QD} is the radius of a flat circular disk. Eq. (12) holds for SET with symmetric junctions.

Today, the number of MOS transistors in the Pentium 4 microprocessor is about 100 millions/cm^2 and the characteristic size of lithography is around 100 nm. Comparing this transistor density with the case of densely packed transistors, we can see that the transistor packing density $\theta = 0.01$, where θ is the ratio of the actual number transistors to the number of devices of the characteristic size at fully dense packing. From Eq. (12), the power dissipation of a chip with N SETs can be given as

$$P_N = N P_1 = N\frac{e^2}{128\varepsilon C_G R_{QD} R} \approx \theta\frac{10^{-4}}{R_{QD}^2}\frac{e^2}{128\varepsilon C_G R_{QD} R} = \frac{10^{-4} e^2 \theta}{128\varepsilon C_G R_{QD}^3 R}. \tag{13}$$

It should be noted that this is the lower limit of power dissipation of the chip because the dissipation of other elements are neglected.

Fig. 4 shows the lower limit of power dissipation (when running at the maximal clock frequency); the maximal clock frequency of the single SET; and the

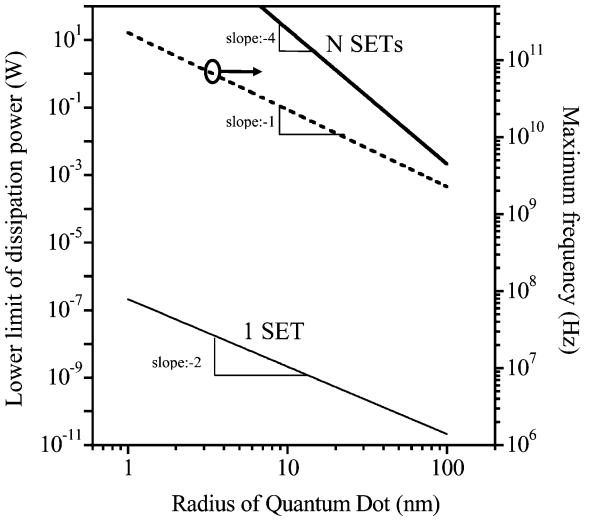

Fig. 4. Lower limit of power dissipation in single electron logic. Power dissipation of a single SET and a chip with N SETs; and the maximal clock frequency; as a function of the radius of the quantum dot. The same packing density $\theta = 0.01$ is supposed as in today's microprocessor chips.

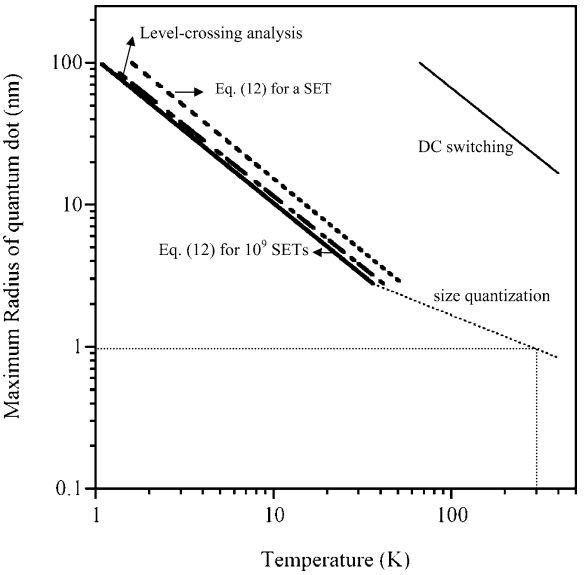

Fig. 5. Maximum radius of the quantum dot for operation at given temperature. The thin solid line represents the requirement of efficient DC switching (on/off) of the device. The other lines give the maximal size for the error-free performance. The dashed line is for a single SET. The rest of the lines are for a chip with 10^9 SETs. The thick solid line is given by Eq. (12), the dashed-dotted line is given by the thermal noise level-crossing analysis [12], and the dotted line estimates the case where the size-quantization effect dominates; it is extrapolated below 2.8 nm.

power dissipation of 10^9 SETs. Here, $\varepsilon = 3.9\varepsilon_0$ for SiO_2, $R = 1$ MΩ and $C_G/C_\Sigma = 0.1$ are assumed. It is apparent from Eqs. (12) and (13) and from the slope of curves in Fig. 4 that $f_{MAX} \propto R_{QD}^{-1}$, $P_1 \propto R_{QD}^{-2}$, and $P_N \propto R_{QD}^{-4}$. It is important to point out that the power dissipation limits of chips, which is today (2003) about 100 W, sets another upper limit for the clock frequency. When the maximal power dissipation of the chip is limited at 100 W, the radius of the QD and the maximal clock frequency are about 6 nm and 30 GHz, respectively. It implies that microprocessors with $R_{QD} \leqslant 6$ nm cannot operate at the maximal clock frequency f_{MAX}. In fact, the maximal clock frequency is less than Eq. (11) due to shot noise [8].

Finally, we study the maximal quantum dot size versus temperature. The results are compared by a simple prediction based on the level-crossing analysis of thermal noise at given capacitance and bandwidth [12]. The rms thermal noise voltage $V_n = \sqrt{k_B T/C_G}$ on the capacitor and the practical noise margin $V_G^{opt} \geqslant 12V_n$ used in [11] yields the following relation:

$$C_G \leqslant \frac{1}{576}\frac{e^2}{k_B T}. \tag{14}$$

In Fig. 5, the thin solid line represents the case where the charging energy is equal to thermal energy, i.e., the device can be used only as a DC switch which is not suitable for error-free data manipulation. Surprisingly, the simple thermal noise estimation works very well at large QD limit. However, as the size of the QD decreases, the size quantization effect becomes dominant.[2] That case has a different slope[3] because $T \propto R_{QD}^{-1/2}$. So, the size quantization effect is a beneficial effect which helps to work at higher temperatures

[2] The radius of the QD is, respectively, 2.77 nm for Si/SiO_2, at which the ratio of energy level spacing in quantum dot to electrostatic charging energy, $E_{QD}/E_C = 4\pi\hbar^2 C_\Sigma/m_e e^2 A_{QD}$ is unit. Here m_e is the effective mass of the electron and A_{QD} is the area of the quantum dot.

[3] The energy level spacing from the size-quantization effect is proportional to $1/R_L^2$, where R_L is the characteristic length of the QD. Since the thermal energy is much less than the spacing between energy levels, the maximum characteristic length of the QD satisfies $\log(R_L)_{MAX} \propto (-1/2)\log T$.

or bigger sizes. The analysis of Fig. 5 suggests that a microprocessor including 10^9 SETs with smaller than 1 nm QD size can work at room temperature.

4. Summary

The aspects of power dissipation and error-free performance have been studied versus the radius of quantum dot (QD). The analysis shows that microprocessors with silicon QDs of less than 1 nm radius can be used at room temperature in single electron logic microprocessors. The most important conclusion is that a single electron microprocessor working at room temperature has to be in the size quantization working mode.

It is important to note that we have used various approximations in order to estimate the ultimate higher limit of quantum dot size at the required error rate. Some of the implicit assumptions are as follows:

(i) For the most optimistic estimation, we supposed that higher-order co-tunneling [14] is negligible, even though it can be important in the Coulomb-blockade region, depending on the geometry and the materials used.

(ii) We have not investigated the impact of possible error correcting methods on the results. However, it is important to mention that, at a given number of devices, the Shannon information channel capacity (the bit/second information measure) of the system cannot increase by using error correction. The error rate can be improved but the Shannon information channel capacity will decrease at any kind of error correction.

Acknowledgements

The research has been sponsored by the Army Research Office (ARL/ARO), Office of Naval Research and TAMU Telecommunication Task Force. Comments of and discussions with Alexander Korotkov and Mark Dykman are appreciated.

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