Fluctuation and Noise Letters
Vol. 4, No. 1 (2004) L83–L86

World Scientific
www.worldscientific.com

ERROR RATE IN CURRENT-CONTROLLED LOGIC PROCESSORS WITH SHOT NOISE

JONG U. KIM and LASZLO B. KISH
Department of Electrical Engineering, Texas A&M University, College Station, Texas77843-3128 USA

Received 27 January 2004
Revised 4 March 2004
Accepted 5 March 2004

The error rate in a current-controlled logic microprocessor dominated by shot noise has been investigated. It is shown that the error rate increases very rapidly with increasing cutoff frequency. The maximum clock frequency of the processor, which works without errors, is obtained as a function of the operational current. The information channel capacity of the system is also studied.

Keywords: Shannon information; single electron transistor; nanoelectronics; bandwidth.

1. Introduction

Threshold crossing problems of Gaussian noise are at the core of many stochastic phenomena. Recently, it has been shown to have a key importance at determining the error rate and energy dissipation in computation [1]. They play also a determining role in stochastic resonators in which systems first Frank Moss studied them experimentally. (Note, Moss's original study is unpublished and Ref. 2 is a subsequent experimental work with his coworkers). In this short note, we expand the study published in [1] and investigate fundamental error rates, speed limits and information channel capacity for current controlled logic processors.

2. Error Rate

Consider a processor with current-controlled logic. Suppose that shot noise is the dominant noise source. Similarly to microprocessors with voltage-controlled logic we suppose that, in the best possible case, the noise margin is 60 % of the current that represents the 'on' state.

If the shot noise is a full shot noise, the one-sided power density spectrum of the shot noise is $2Iq$, where I is the current and q the electron charge. For a single gate, Rice's generalized formula [1] of threshold crossing yields the error rate as follows:

$$\nu_f(I, f_c) = \frac{2}{\sqrt{3}} f_c \exp\left(-\frac{9}{100}\frac{I}{f_c q}\right) \tag{1}$$

where f_c is the cutoff frequency, which is roughly equal to the highest possible clock frequency, of the microprocessor. Eq. (1) implies, see Fig. 1, that the error rate increases very rapidly with increasing cutoff frequency.

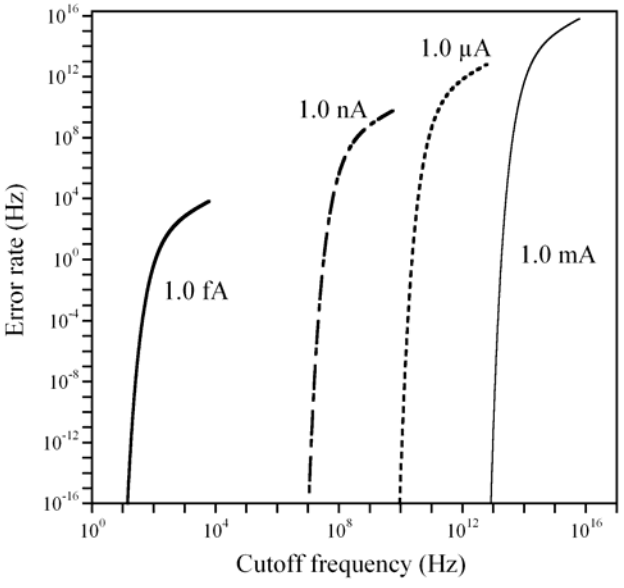

Fig. 1. Error rate of a single transistor in the processor. Each number represents the 'on' state current.

A reasonable assumption for the upper limit of acceptable noise-induced bit error rate (maximal error rate) is one error/chip /year, i.e., $f_{year} = 3.17 \times 10^{-8}$ Hz [1]. Eq. (1) implies that the maximum cutoff frequency (maximal bandwidth), $f_{c,max}$, in a processor with N transistors is given by[a]:

$$f_{c,max} = \frac{\sqrt{3}}{2} \frac{f_{year}}{N} \exp\left[w\left(\frac{3\sqrt{3}}{50} \frac{I}{q} \frac{N}{f_{year}} \right) \right] \tag{2}$$

where $w(x)$ is the Lambert W-function [3]. Since the Lambert function, $w(x)$, can be approximated by $\ln x - \ln(\ln x)$ for $x >> 3$, the maximal bandwidth can be given as follows:

[a] Equation (1) at $v_f = f_{year} / N$ is also solved by numerical method. The maximum cutoff frequency obtained by bisection method gives the same as by Eq. (2). The values of the Lambert W-function are evaluated in Matlab. Figs. 2 and 3 are plotted on the basis of Eq. (2).

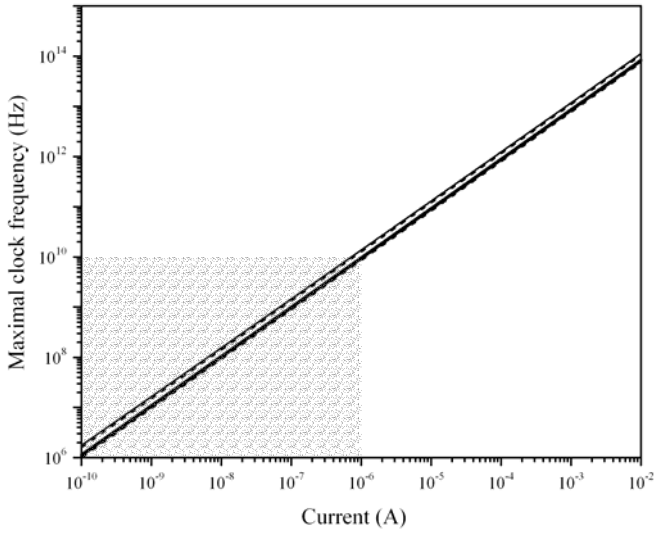

Fig. 2. Maximal bandwidth, $f_{c,max}$, of the processor that works with the maximal error rate. The solid lines are the exact numerical solution of Eq. (1) and the dotted lines are from Eq (2). The thin line (upper lines) represent the case of one transistor and the thick ones (lower lines) represent the processor with 10^8 transistors. The shaded area is the possible range of operation with 10^8 transistors and 100 Amp upper limit of the supply current.

$$f_{c,max} \approx \frac{9}{100}\frac{I}{q}\left[\ln\left(\frac{3\sqrt{3}}{50}\frac{I}{q}\frac{N}{f_{year}}\right)\right]^{-1} \tag{3}$$

Figure 2 shows $f_{c,max}$ as a function of the operation current. The $f_{c,max}$ function is a good estimation of the maximal clock frequency of the processor with the maximal error rate. Thus thin solid line represents the maximal clock frequency of the single element and the thick solid line represents that of a microprocessor with 10^8 elements. It is apparent that the maximal clock frequency is almost independent of the number of the elements in the processor.

The information channel capacity C of a single channel is given by Shannon information formula:

$$C = B\ln\left(1 + P_{signal}/P_{noise}\right) \tag{4}$$

where B is the bandwidth of signal, which can be approximated by the clock frequency in the logic processor; and P_{signal} and P_{noise} are power of signal and of noise, respectively. Since the signal is a square wave, P_{signal}/P_{noise} can be approximated as the ratio of the clock frequency and the error rate. Supposing the all transistor process independent and useful information, the upper limit of information channel capacity can be written as:

$$C = N\, f_{c,max} \ln\left(1 + \frac{f_{c,max} N}{f_{year}}\right). \tag{5}$$

Figure 3 shows the information channel capacity at the maximal clock frequency. As shown in Fig. 2 and Fig. 3, the maximum clock frequency and the information channel capacity increase monotonically with increasing the operation current. The shaded area is the possible range of operation if the maximal supply current is 100 Ampere.

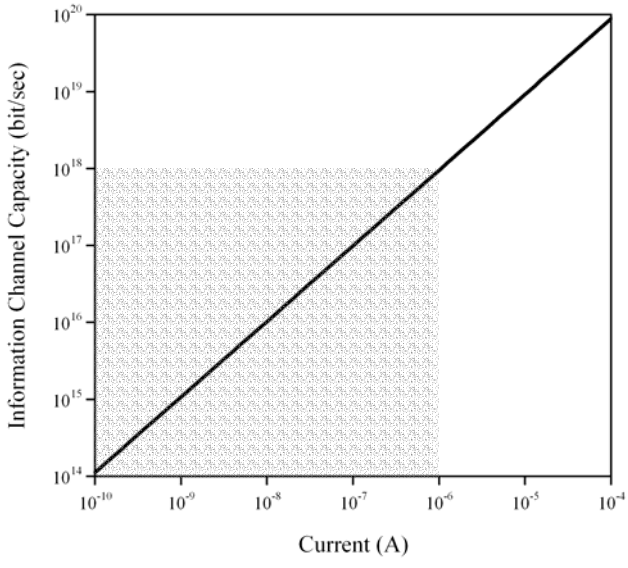

Fig. 3. Upper limit of information channel capacity at the maximum clock frequency. The thin solid line represents the one transistor and the thick the processor including 10^8 transistors. The shaded area is the possible range of operation with 10^8 transistors and 100 Amp upper limit of the supply current.

3. Summary

The study shows some fundamental limits of information processing in current controlled logic with shot noise. With 100 million transistors, such as Pentium 4, and with the assumption of a maximal supply current of 100 A, the highest clock frequency would be 10 GHz.

Acknowledgements

The research has been founded by the Army Research Office and the Office of Naval Research.

References

[1] L. B. Kish, *End of Moore's law: thermal (noise) death of integration in micro and nano electronics*, *Phys. Lett. A* **305** (2002) 144–149.
[2] Z. Gingl, L.B. Kiss and F. Moss, *Non-dynamical Stochastic resonance*, *Europhys. Lett.* **29** (1995) 191.
[3] N. G. de Bruijn, *Asymptotic Methods in Analysis*, 2nd Ed., North-Holland Publishing, Amsterdam (1961) 25–28.